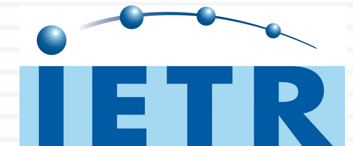
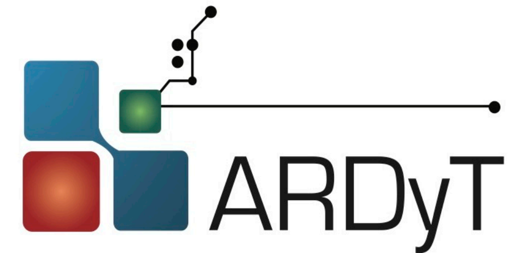


Projet ANR ARDyT



Architecture Reconfigurable dynamiquement Tolérante aux fautes

Sébastien Pillement – IETR SCN

INS

Réunion ISIS – 2 juillet 2013

ARDyT

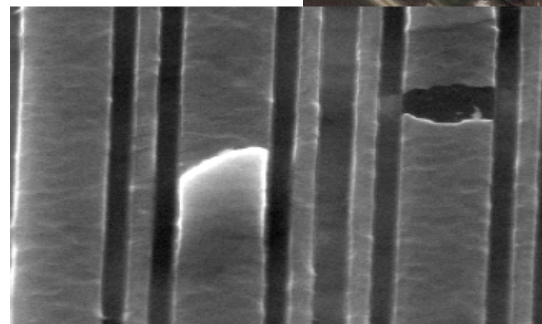
Plan

- Introduction et contexte
- Approche architecturale
  - Protection des ressources de bases
  - Protection des blocs arithmétique
  - Protection du bitstream
- Approche système
  - Gestion dynamique
- Approche niveau outils
- Conclusion

ARDyT

Conjonction de deux phénomènes

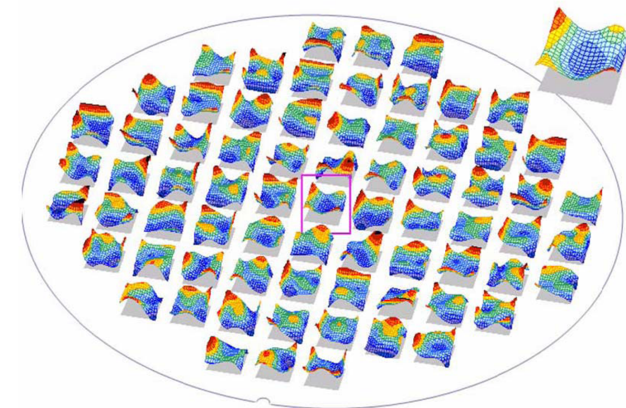
- de plus en plus de systèmes sont critiques.
  - Espace, Aviation, médical, automobile,
  - Banque, militaire,
  - Contrôle commande, …
- Evolution technologique
  - Technologies nanométriques
  - Erreurs permanentes
  - Erreurs transitoires

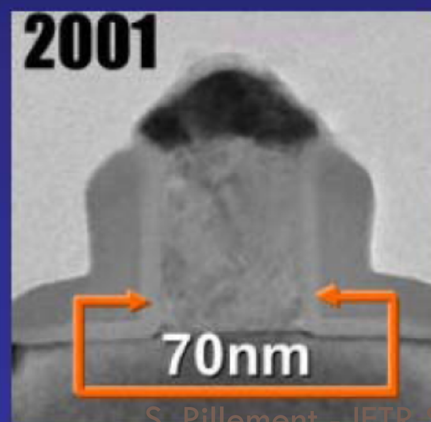


Cadence cdn LIVE India 2007

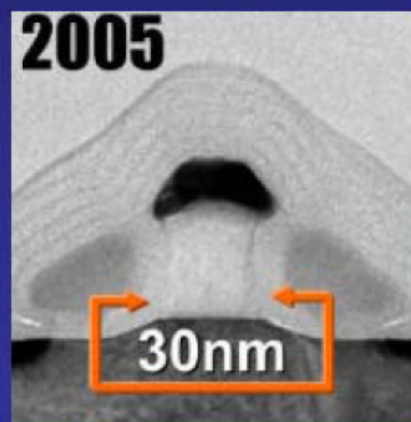
Erreurs permanentes

- Défauts de fabrication
- Dispersion des paramètres
- Vieillissements
- Stress électrique

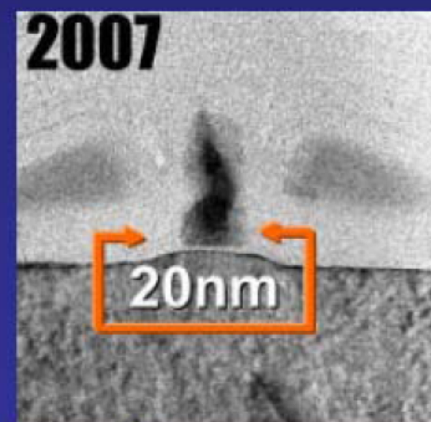




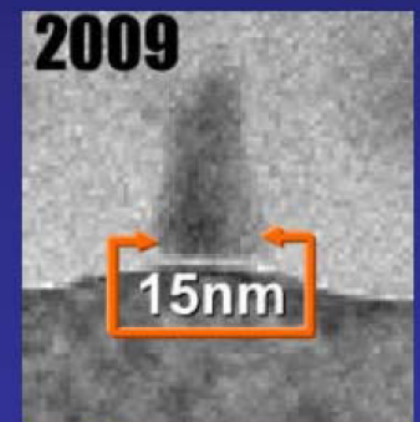
0.13u process



65nm process



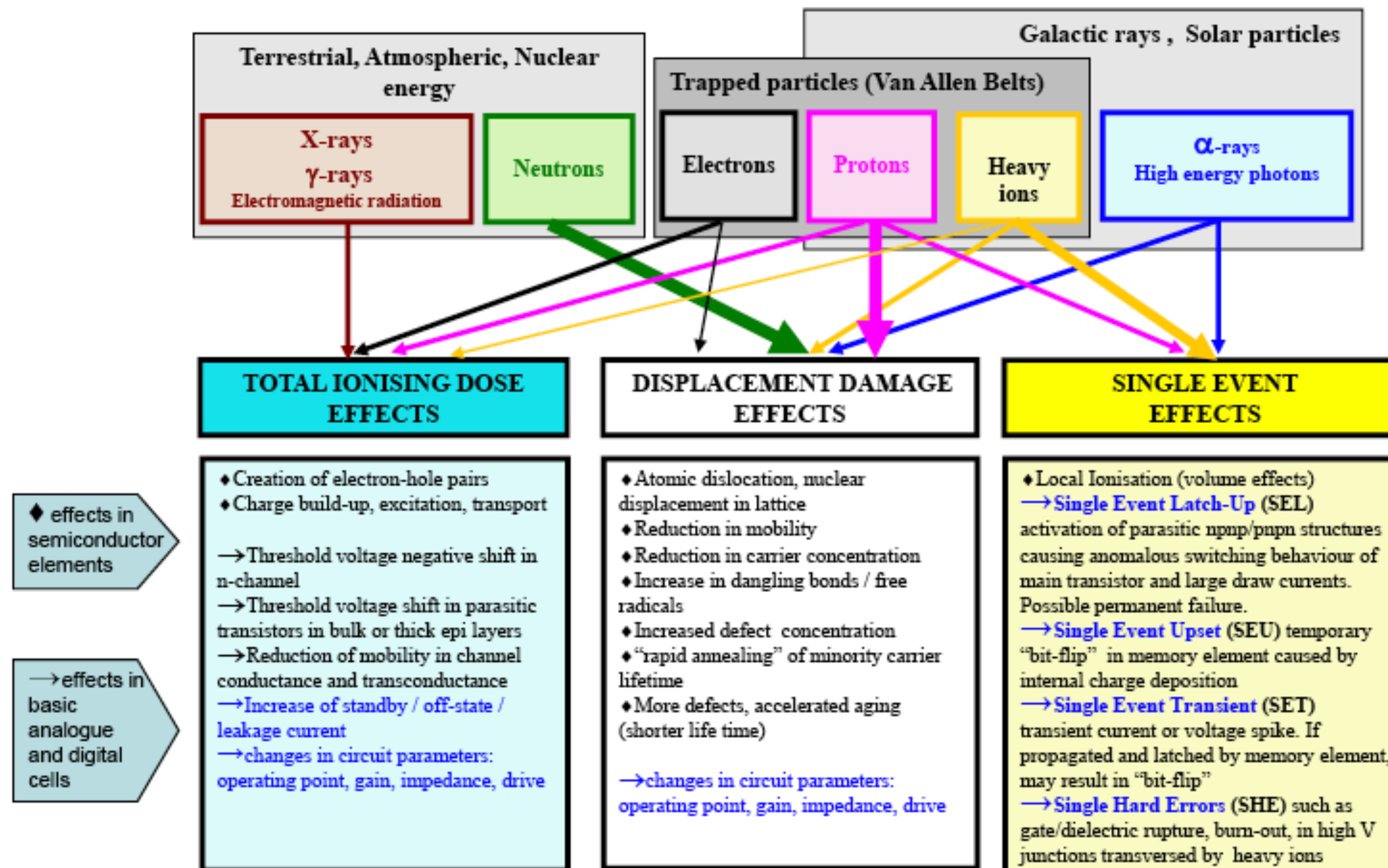
45nm process



32nm process

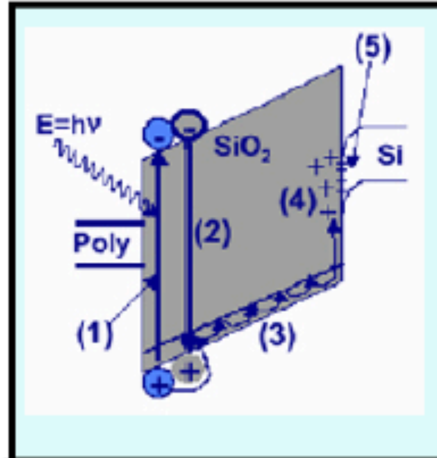
Sources de radiations

5



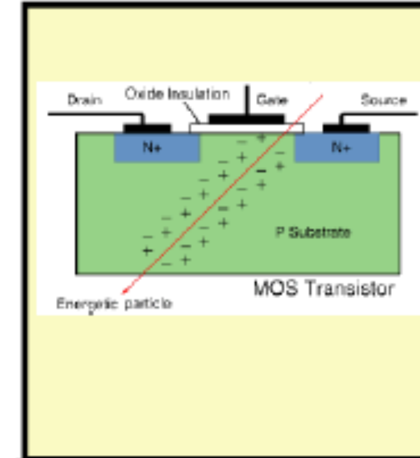
Impact des radiations

TOTAL IONISING DOSE EFFECTS	DISPLACEMENT DAMAGE EFFECTS	SINGLE EVENT EFFECTS



Typically this only concerns

electro-optic sensors, diodes, opto-couplers, solar cells, wide-base bipolar transistors



→potential effects at ASIC or FPGA level

- POWER CONSUMPTION INCREASE
- DEGRADATION OF ANALOGUE FUNCTIONS / PERFORMANCE

- TEMPORARY OR PERMANENT MALFUNCTION
- LOSS OF DATA
- POWER CONSUMPTION INCREASE
- DEVICE BURN OUT

Evénements singuliers

- Mise en route d'un transistor parasite PNP dans un MOSFET (SES - Single Event Snapback).
- Mise en conduction d'un thyristor parasite ou latch-up (SEL - Single Event Latch-up)
- Destruction du composant (SEB - Single Event Burn-out).
- Rupture de la grille des transistors MOS (SEGR-Single Event Gate Rupture)

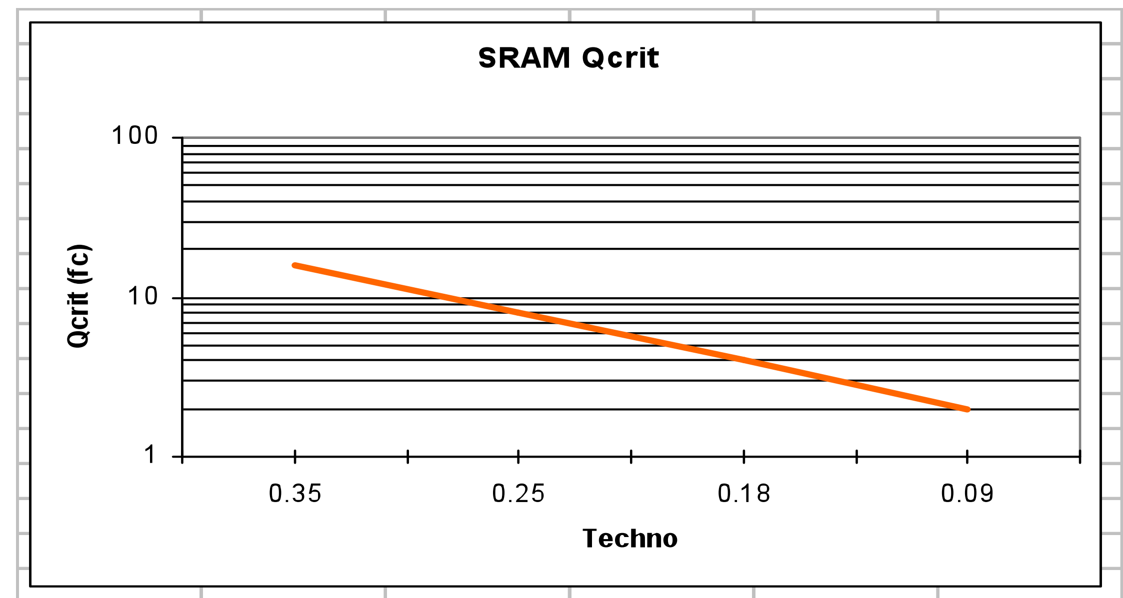
Destructif

- Basculement aléatoire d'une fonction bistable (SEU - Single Event Upset) Soft errors

Effet au sol

- Avec la réduction de la technologie, les radiations ionisantes deviennent un problème au sol

- Définitions :
  - Qcrit = charge critique = Niveau de charge nécessaire pour déclencher un événement
  - FIT = Taux d'erreurs (Failure in Time) = Fréquence d'erreurs causées par les radiations
    - 1 FIT = 1 erreur pendant 10^9 heures,
    - 1000 FIT = 1 erreur sur 114 ans



Effet sur des mémoires

- Campagne de test sur 80 mémoires en technologie CMOS 0.13um (Dec 02)

Conditions	FIT/Mb Neutrons	FIT/Mb alpha Am241	TOTAL
Sea level	1300	2200	3500
Alt.1500 m	3000	2200	5500

- Mesures Alpha varient drastiquement en fonction du type de package
- Pour 128 Mo, 1 erreur tous les 14 jours au niveau de la mer

Field Programmable Gate Array (FPGA)

"Field Programmable"

- Integrated Circuit(IC) designed to be configured by the customer .

Why do we need FPGA ?

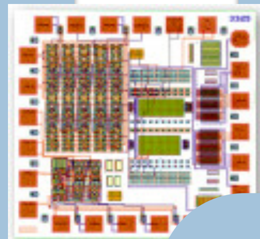
- ✓ Design Flexibility
- ✓ Partial Re-Configuration
- ✓ Low Non-Recurring Engineering Cost
- ✓ Fast Time to Market

ARDyT

The reconfiguration opportunities

Self-repair

- overcome effects of threats & environment
- improve reliability lifetime
- graceful degradation



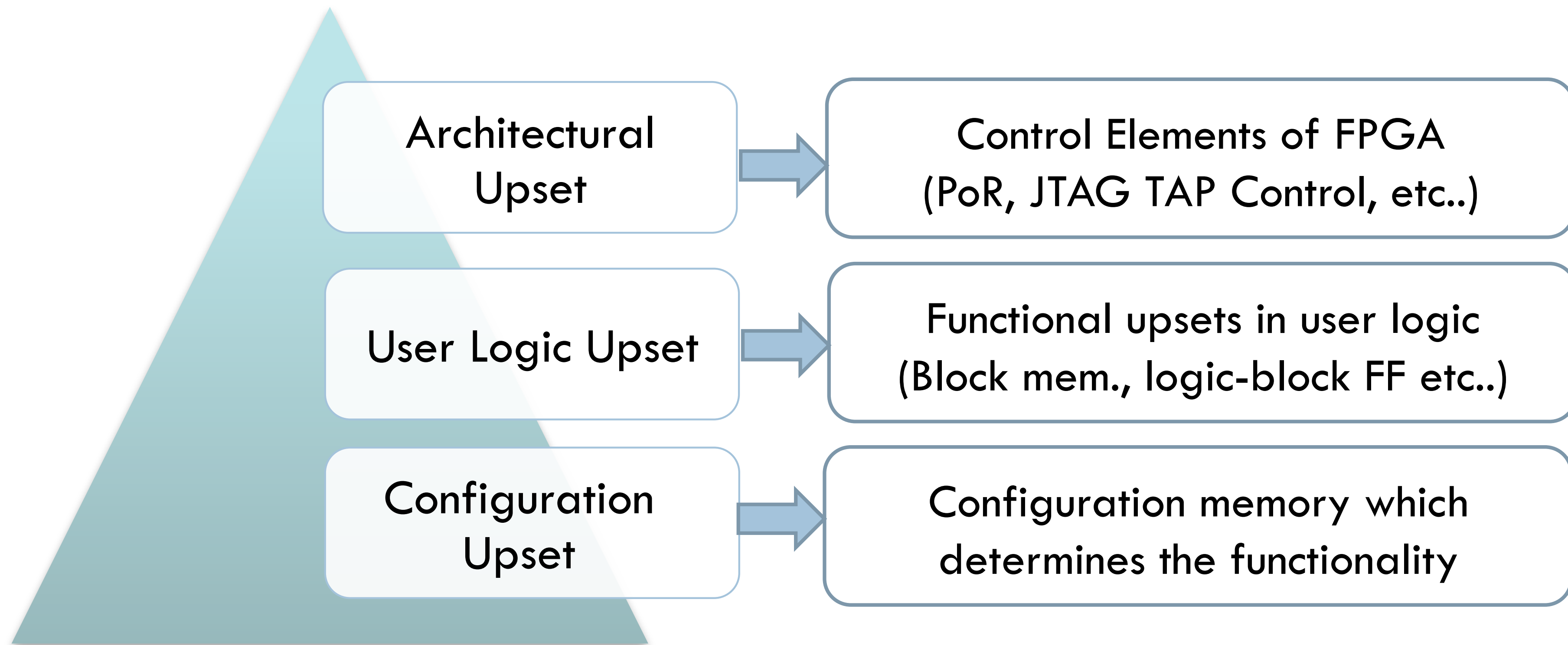
Reduce deployment time

- adaptive interfaces to facilitate spacecraft integration
- reduce parts variety

Adapt to evolving threats, missions, & environments

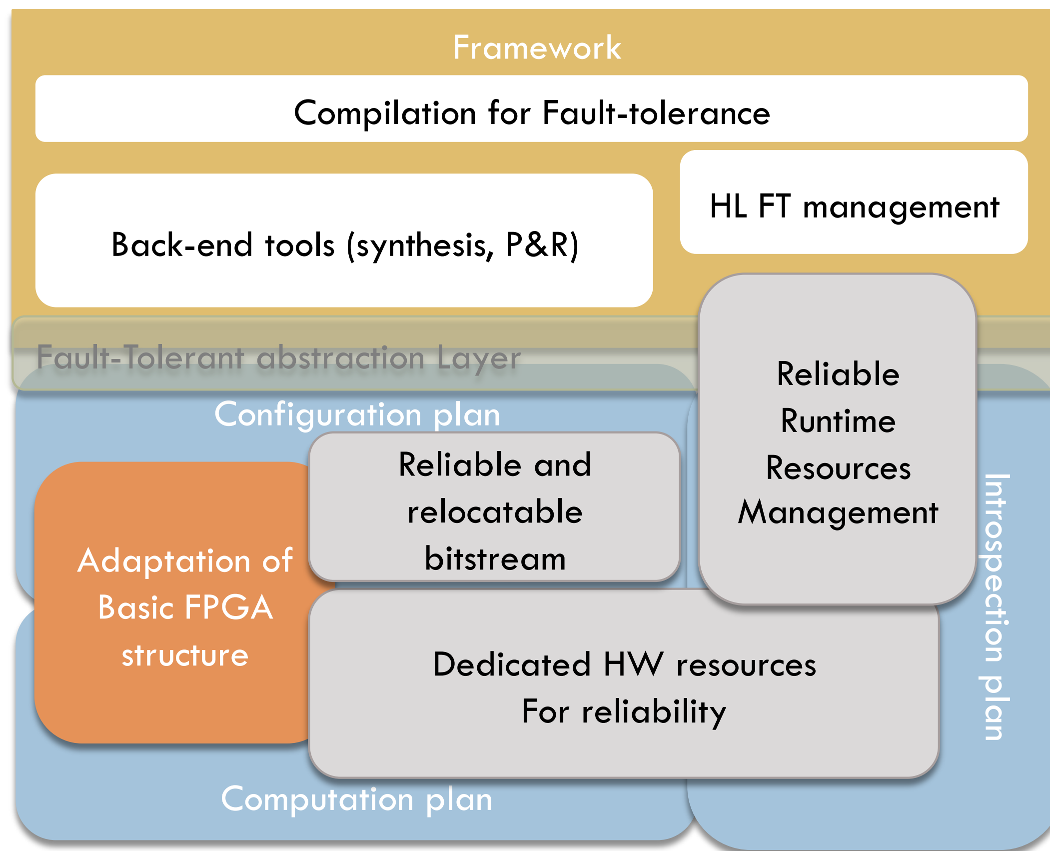
- self-optimizing, high performance
- reconfigurable functionally
- redefinable power & data pathways

Upset Categories in FPGA



Hardened circuits at high costs and loss in performances

The ARDyT approach



- Architecture
  - Basic FPGA blocks protection
  - Bitstream protection
  - Dynamicity support
- System
  - Dynamic management
- Tools
  - DFFT

ARDyT

Plan

- Introduction et contexte
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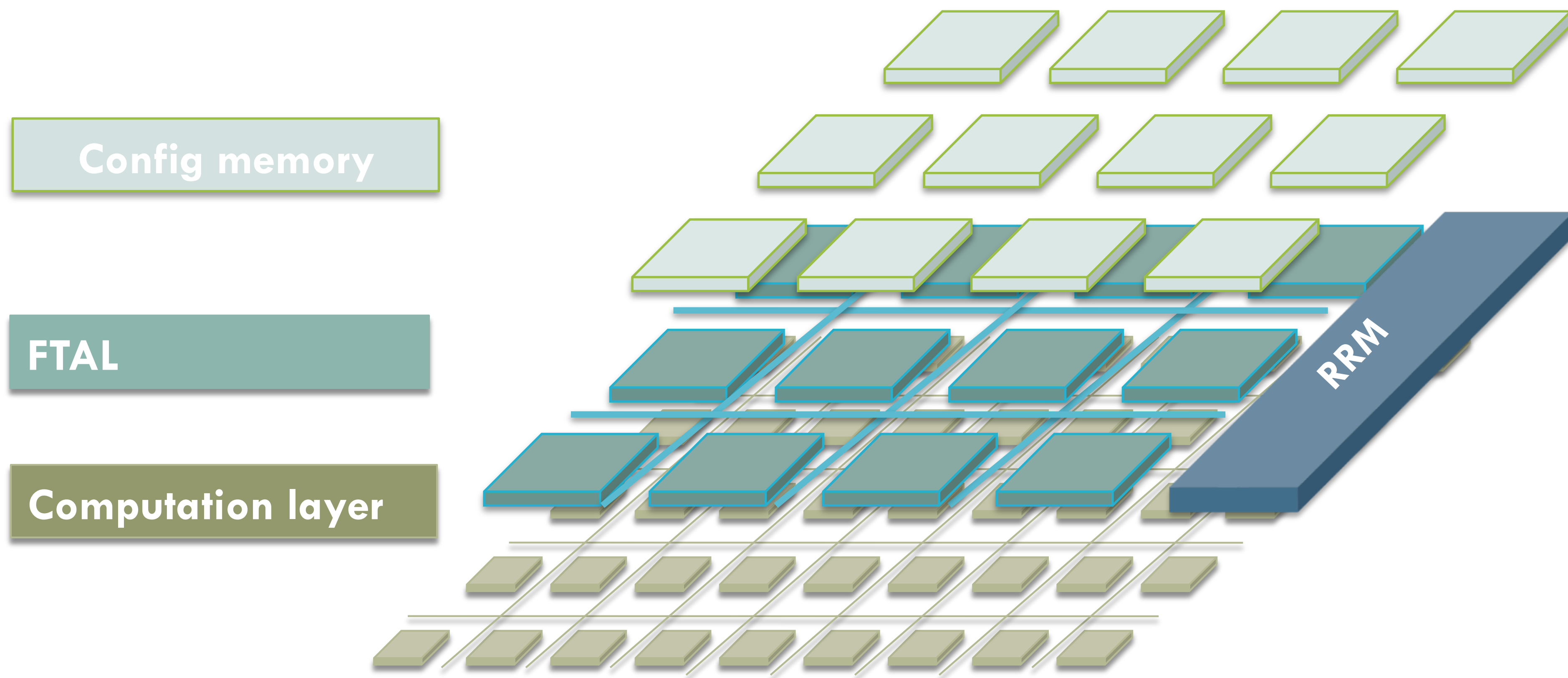
System architecture



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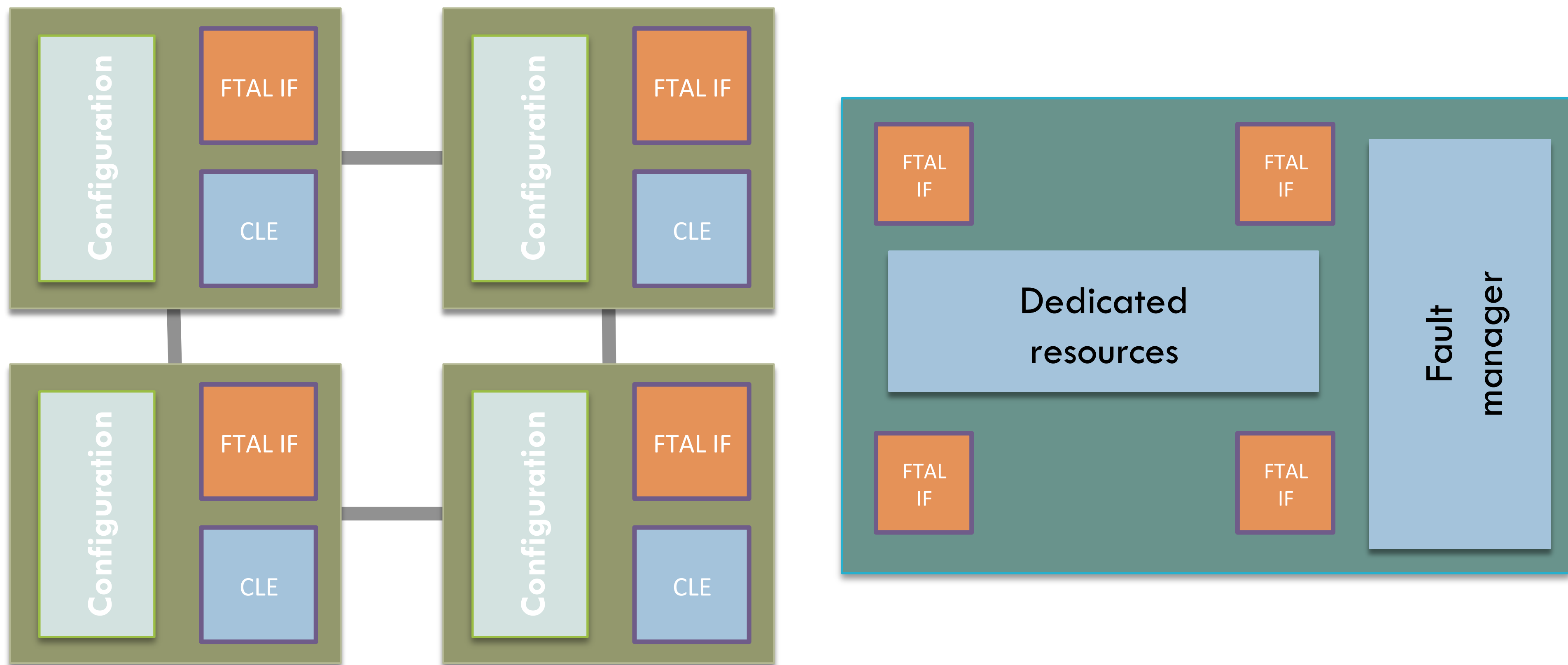
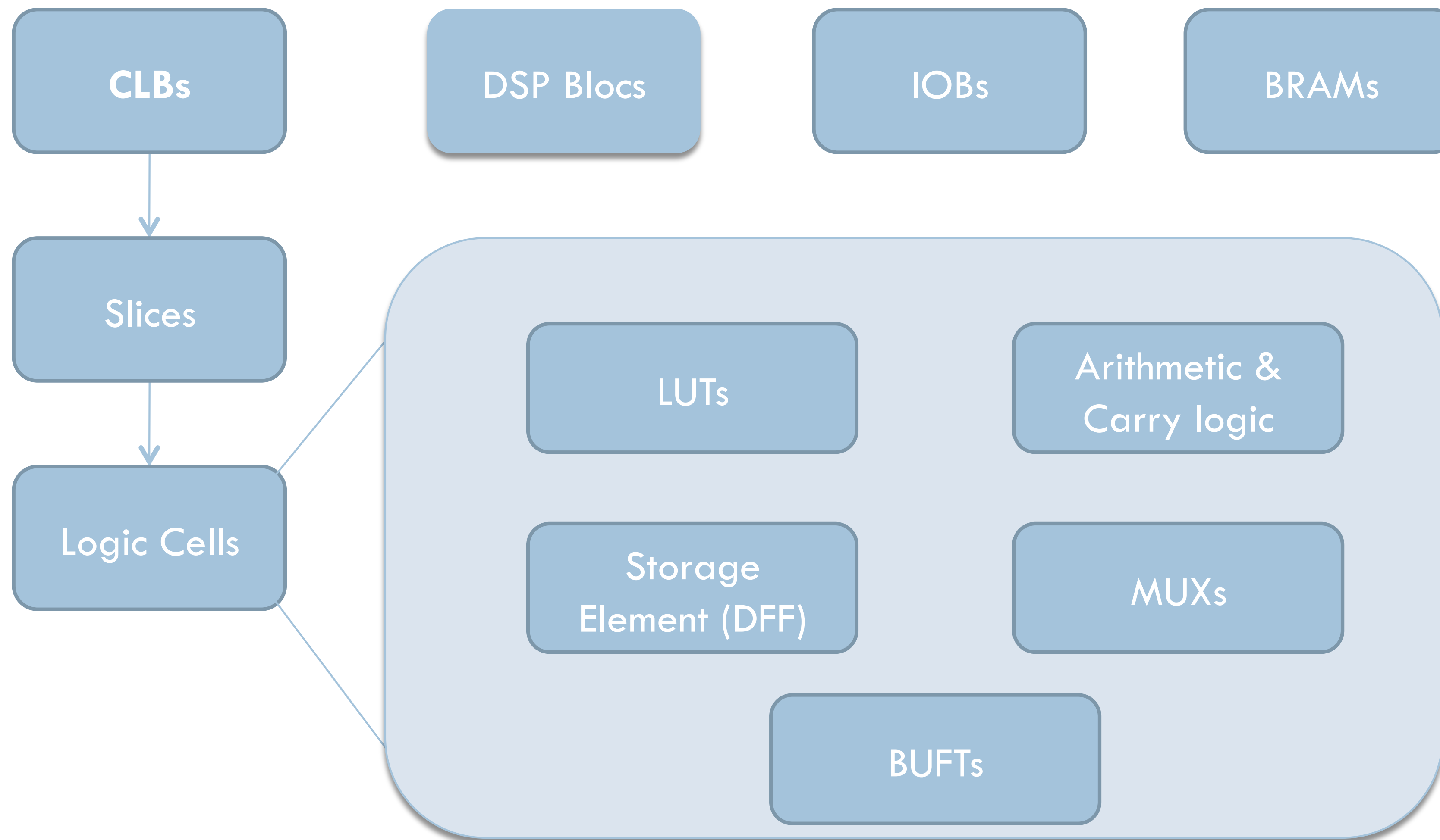
Architectural model



Types of CLE (Xilinx taxonomy)



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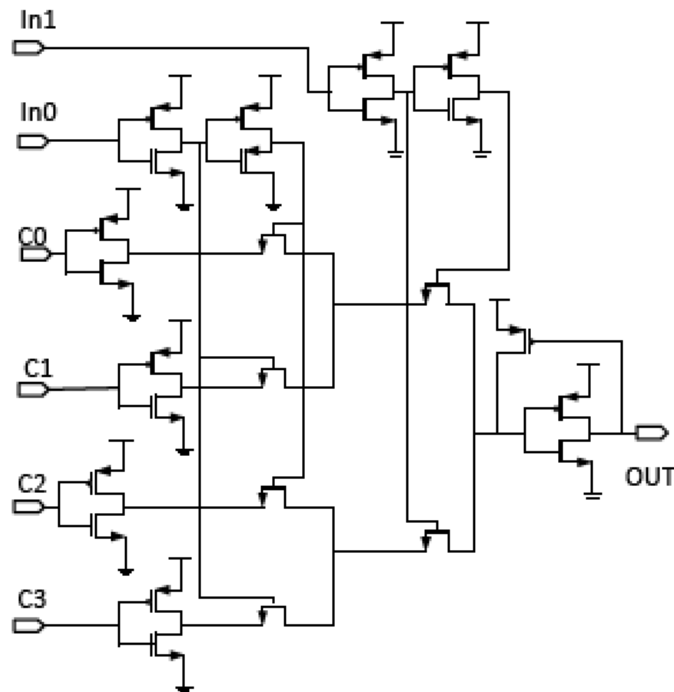
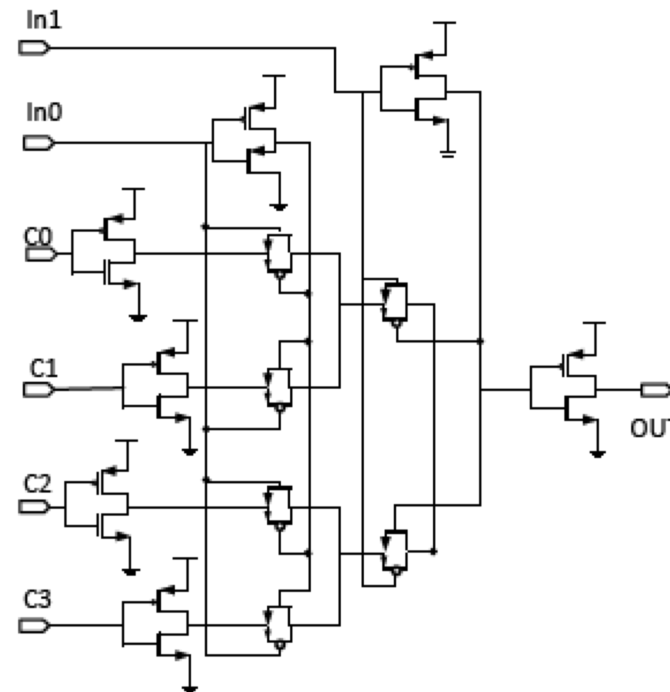
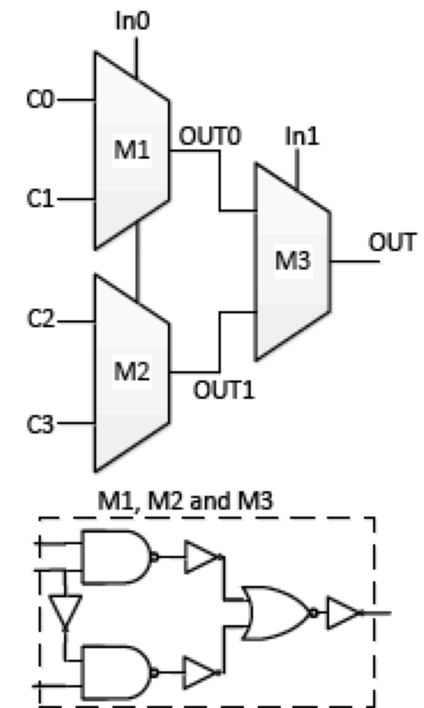
LUT protection







- Most reliable structure?
- Wear-out mitigation by input swaping and « don't care » use.

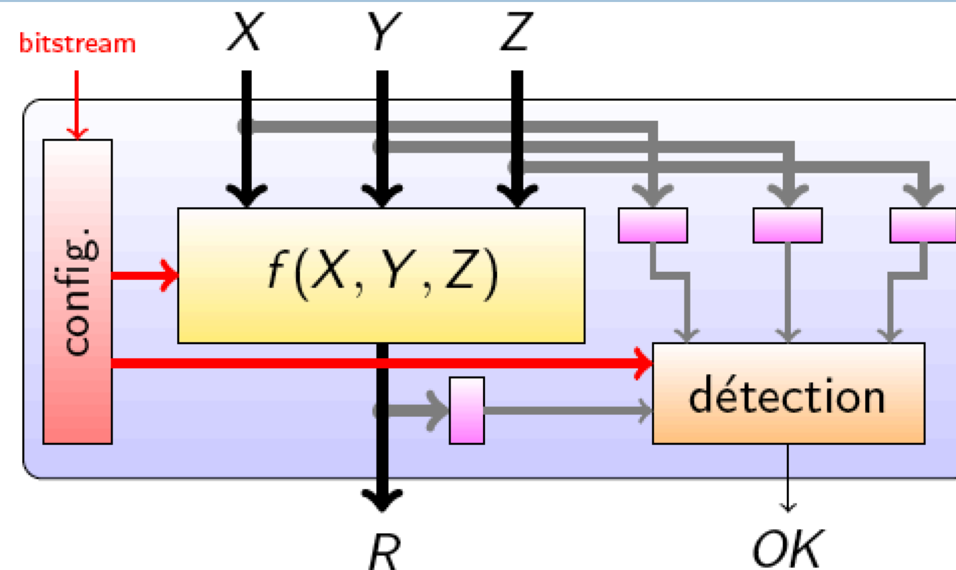
DSP block protection

Opérations supportées :

$$R \leftarrow X \cdot Y \pm Z$$

avec configurations :

- X, Y sur 8, 12, 16 bits
- Z sur 16, 24, 32, 40 bits
- signés / non-signés



Exemples résultats implantation ASIC 130 nm pour délai de 4 ns :

moduli	surface (μm^2)			puissance dyn. (μW)		
	comb.	reg.	total	cellules	noeuds	total
$\{2^6, 13, 15, 17\}$	12 068.9	10 983.7	23 052.6	1 734.9	293.4	2 028.3
$\{2^5, 13, 15, 31\}$	12 020.5	10 915.0	22 935.6	1 723.1	290.8	2 013.9
$\{2^3, 7, 13, 15, 17\}$	12 037.5	12 018.7	24 056.2	1 830.5	332.3	2 162.8
$\{2^2, 7, 13, 15, 31\}$	12 478.7	11 555.6	24 034.3	1 820.7	331.5	2 152.2
$\{2^2, 7, 15, 17, 31\}$	13 079.5	12 224.2	25 305.8	1 910.4	304.7	2 215.1

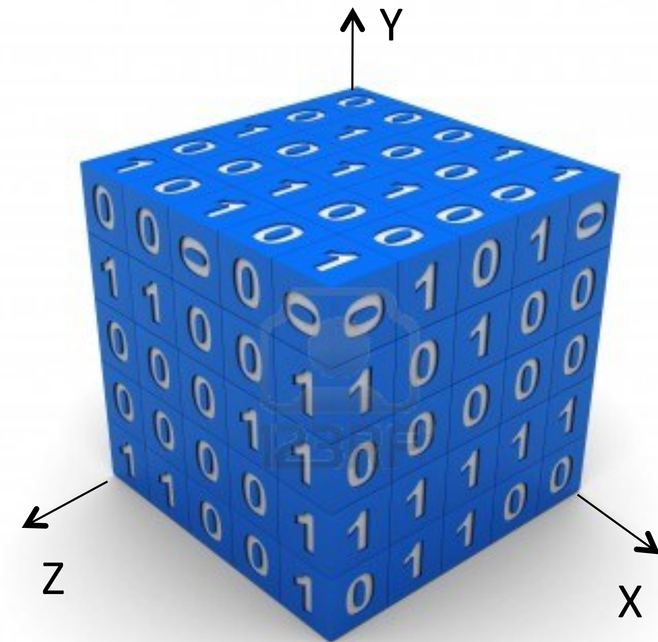
Configuration Memory Protection

3-Directional Hamming Scheme (3DH):

- A Built-in 3 Directional Hamming Error Correcting Mechanism is proposed.
- Mainly for Configuration memory protection.
- Doesn't need the backup copy (golden copy*) of whole configuration memory.
- Excessive access delay via IO ports is avoided.

Functionality:

- Information need to be protected is arranged in a memory platform.
- Hamming error correcting mechanism is applied to data words of the cube in all 3 directions (X, Y and Z).
- Maximum error bits are corrected.
- Multi-bit Upsets (MBUs) are easily cleared in this scheme.



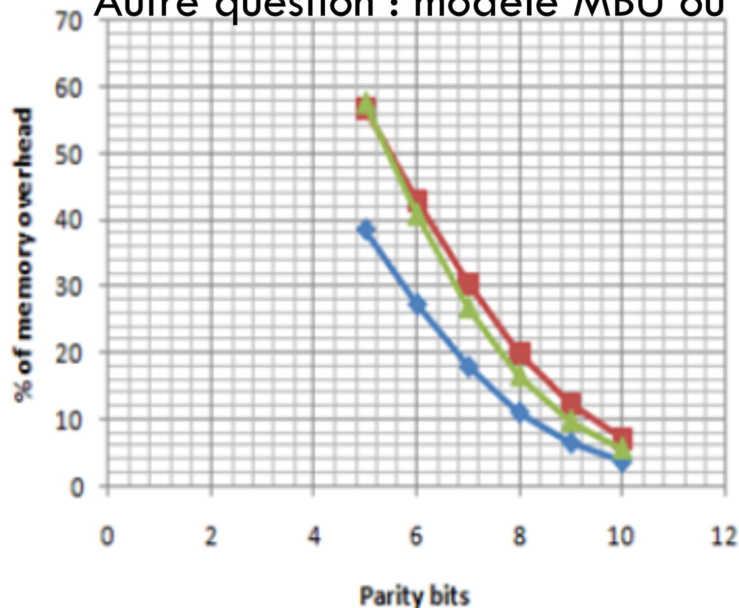
Requirements of 3DH:

- A virtual or physical 3D memory platform.
- Additional hardware or software to perform Hamming error correction on the 3D cube.
- Additional memory space to keep parity check bits of Hamming computation.

Question ici sur les conditions de mesures ? Combien d'erreurs ?? Pattern de fautes ?

Computational Results:

Autre question : modèle MBU ou SBU ? Bertrand à un article et une table excel d'évaluation from Xi



Comparison of parity memory overhead.

NON CORRECTABLE ERROR PATTERN COMPARISON

Window size	1DH scheme		2DH scheme		3DH Scheme	
	T_b	$\%N_{ep}$	T_b	$\%N_{ep}$	T_b	$\%N_{ep}$
3	3	0.5	9	0.1718	27	0.0086
4	4	0.6875	16	0.2368	64	0.0060

T_b - Total bits protected ; $\%N_{ep}$ - % of non correctable error patterns

Conventional 1D Hamming
Conventional 2D Hamming
Proposed 3D Hamming

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Bitstream protection

- Dynamic reconfiguration
  - Needs to support partial reconfiguration
- Relocatable bitstream
  - Enable task migration
- Bitstream encoding
  - Uses of adapted encoding
  - « Verifiable » bitstream

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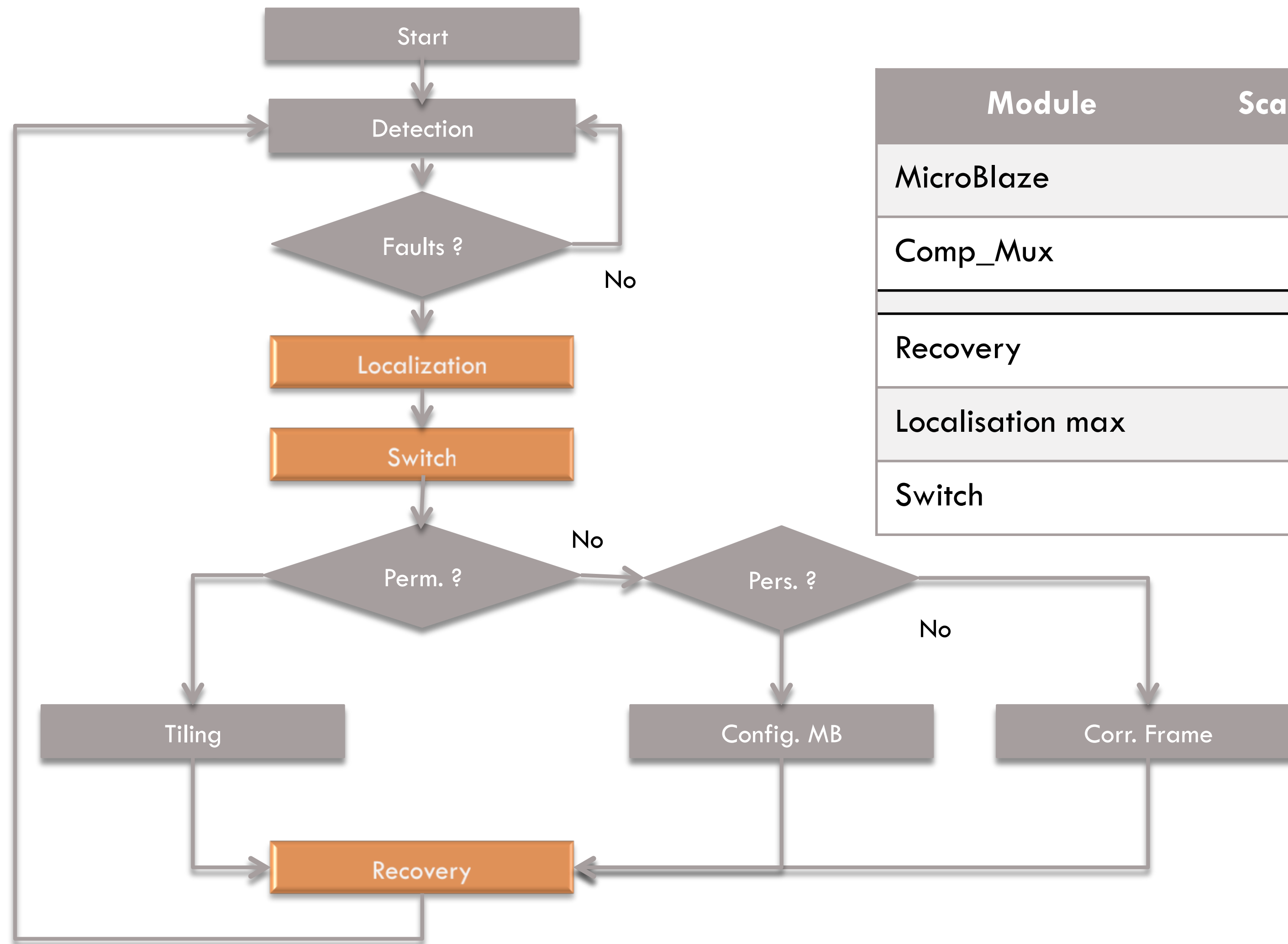
Runtime Reliable Manager

- Dynamic reconfiguration capabilities
- Data-stream management capabilities
- Optimization of processing execution able to match functional requirements even under faulty conditions
- Efficient management system able to modify and adapt available FPGA resources (changing due to faults) during execution

- Based on fault detection mechanisms implemented in the hardware

Implement the fault mitigation strategy

Fault mitigation technique



Module	Scan time (µs)	Reconf time (µs)
MicroBlaze	270	326 000
Comp_Mux	25	185
Recovery	N/A	5,2
Localisation max	N/A	300
Switch	N/A	0,002

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Approche outils

- Modeleur d'architecture virtuelle

Conception d'un plan d'introspection dans la couche virtuelle

Plan de configuration + Plan d'introspection

Contrôleur de configuration

Plan de calcul

Couche Virtuelle

Couche matérielle

- Prise en compte de ressources sous forme d'IP
- Paramétrisation du bitstream
- Adaptation des outils d'exploitation
- Mise à disposition des outils

- Outillage d'exploitation

Exploration

Intégration

Description matérielle (DSL)

Modèle Opérateur

Génération

Exploitation

Application

Modèle Architecture

Placement Routage

Génération

Bitstream

Architecture VHDL

Flot de conception

Synthèse

Outil commercial

Cible matérielle

Emulation

ARDyT

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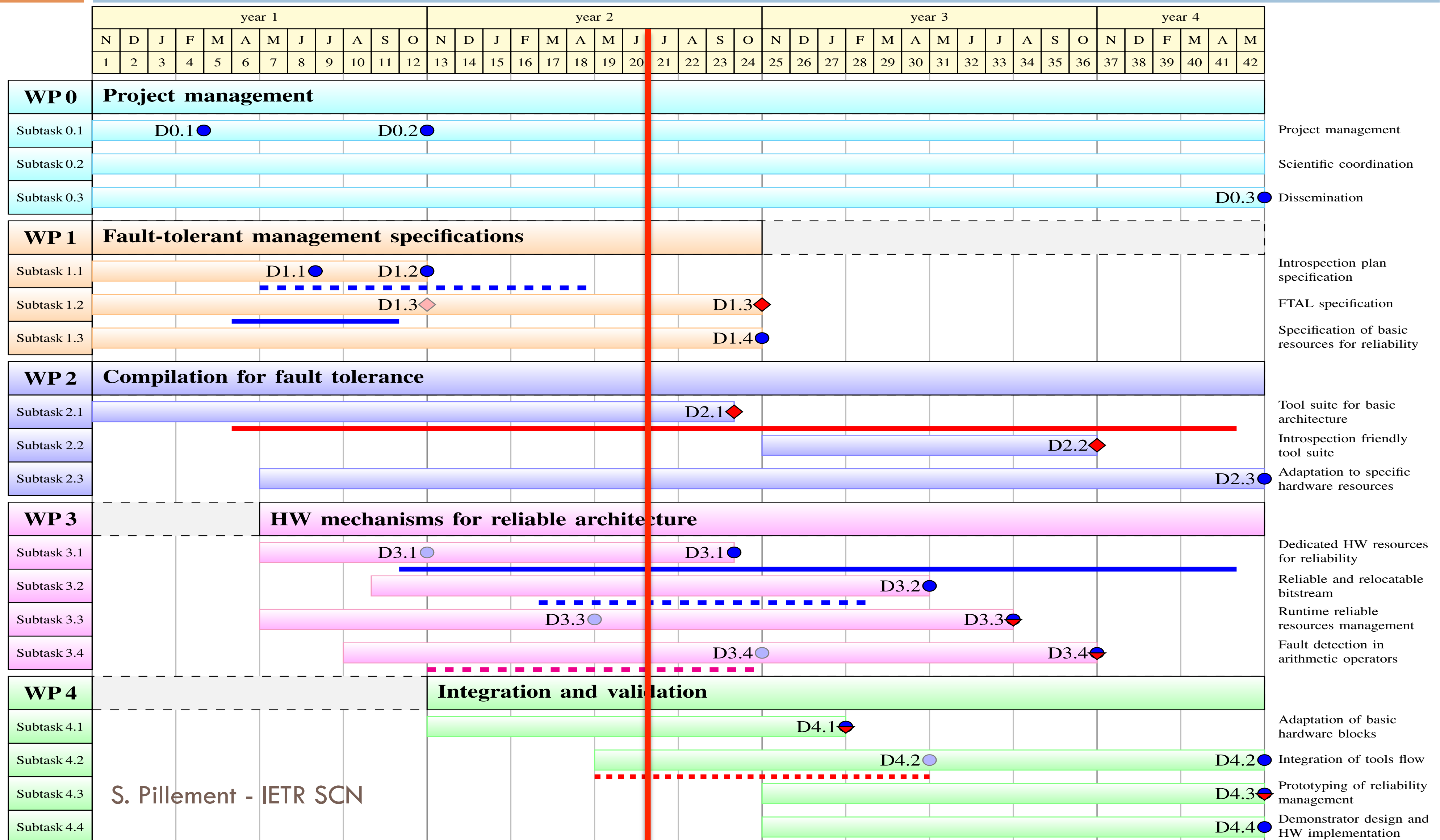
ARDyT

Le projet ARDyT c'est ...

Implémenter efficacement des applications dynamiques sur une architecture flexible, sûre et faible coût

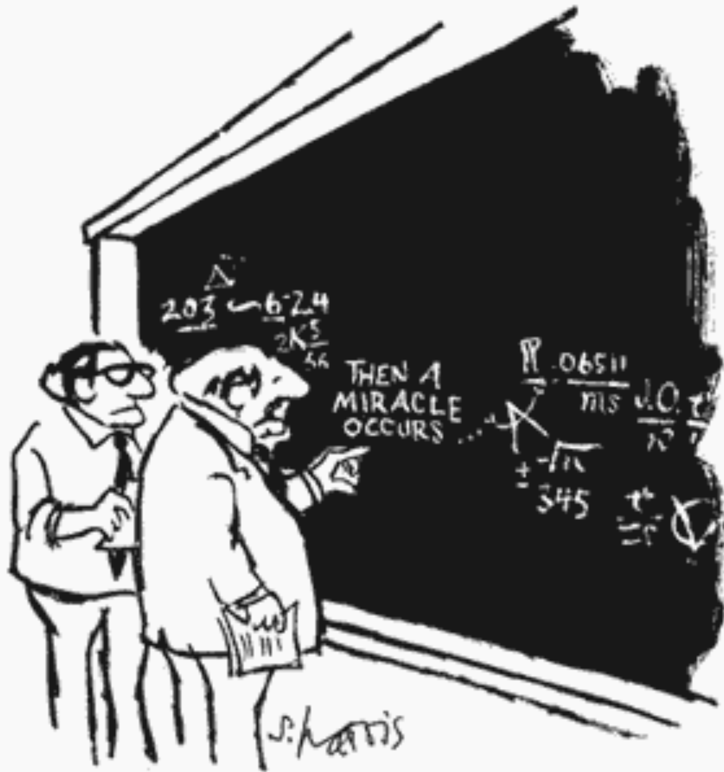
- Principaux verrous
  - Structure matérielle « fiable »
  - Gestion dynamique de la fiabilité
  - Outils pour la fiabilité
- Innovations
  - Couche d'abstraction tolérante aux fautes
  - Gestion de la reconfiguration tolérante aux fautes
  - Approches arithmétiques et codage au niveau circuit
  - Synthèse pour la fiabilité sur le plan d'introspection
  - Tolérance aux fautes dynamique (self-healing)

Time schedule



What's next

- Architecture
  - Routing protection
  - User memories
  - DSE on DSP blocks
  - Use of exotic arithmetics
- System
  - Design of Reliable Ressources Manager
  - FTAL specification
- Tools
  - Design for Fault-tolerance
  - Introspection plan



Ardyt.irisa.fr

Merci de votre attention.

Question ?

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