

An Overview : Dynamically Reconfigurable Fault Tolerant FPGA Architecture

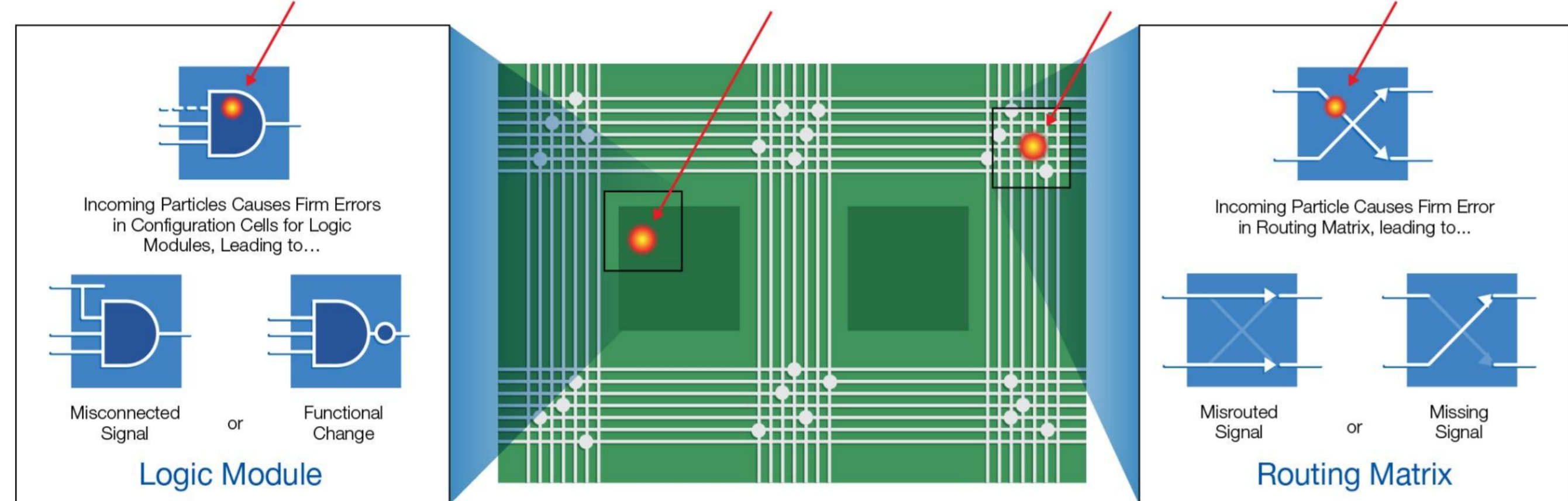
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1 Radiation Susceptibility of SRAM Based FPGA



a) Consequences of Configuration Upset

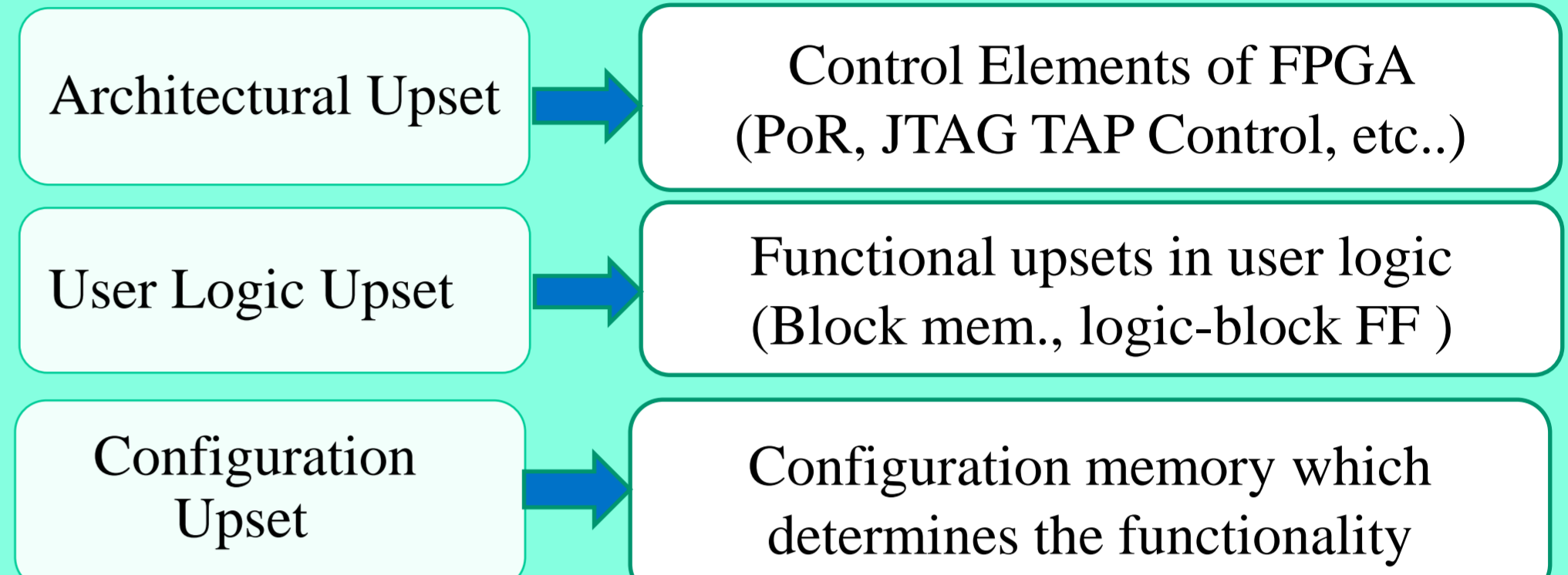
Recoverable Effects:

SET – Single Event Transients
SEU – Single Event Upset
SBU – Single Bit Upset

Recoverable Effects:

SEL – Single Event Latch Ups
SEB – Single Event Burnouts
SEGT – Single Event Gate Rapture.
SEFI – Single Event Functional Interrupts

Physics same but Observability and Consequences vary.



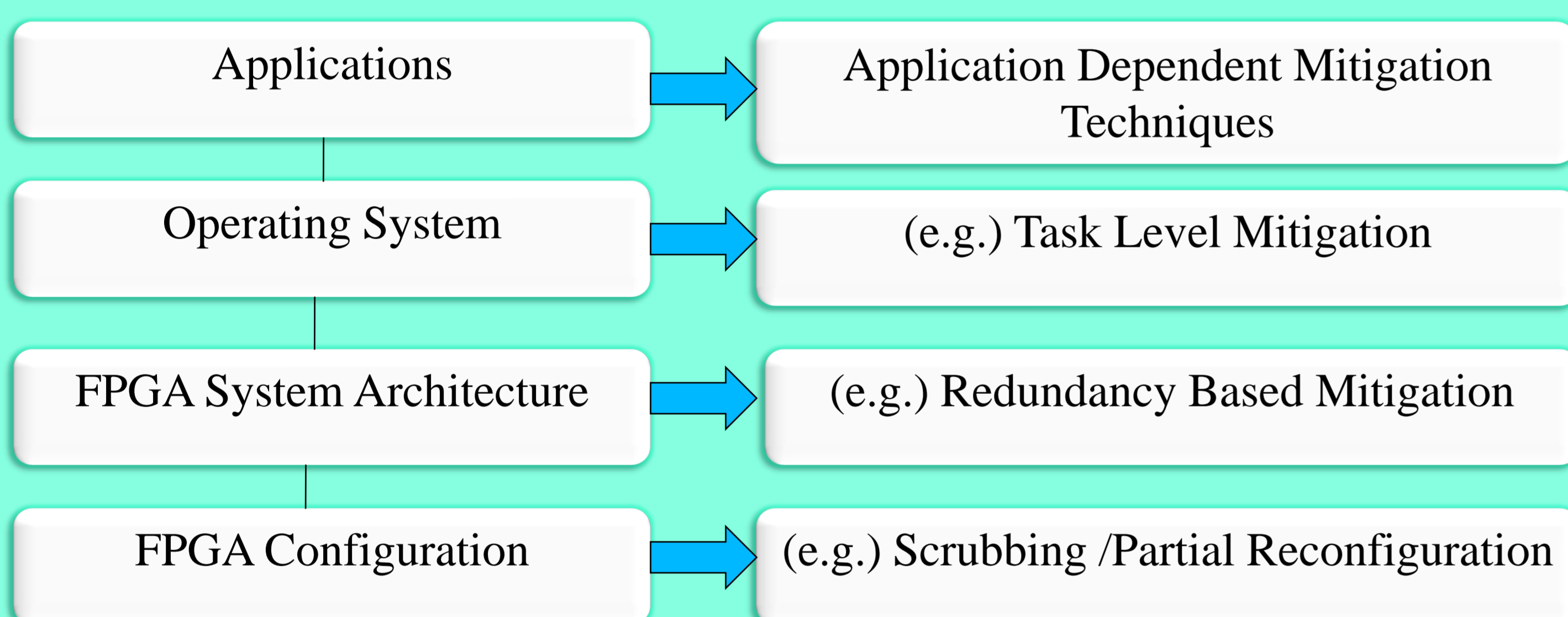
b) Upset Categories in FPGA

*SRAM - Static Random Access Memory

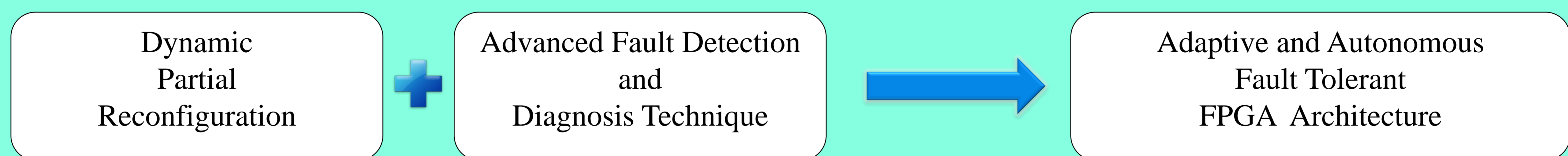
*FPGA – Field Programmable Gate Array

2 Multilayer Fault Mitigation

Distributing the task of fault mitigation at different layers of the FPGA system.

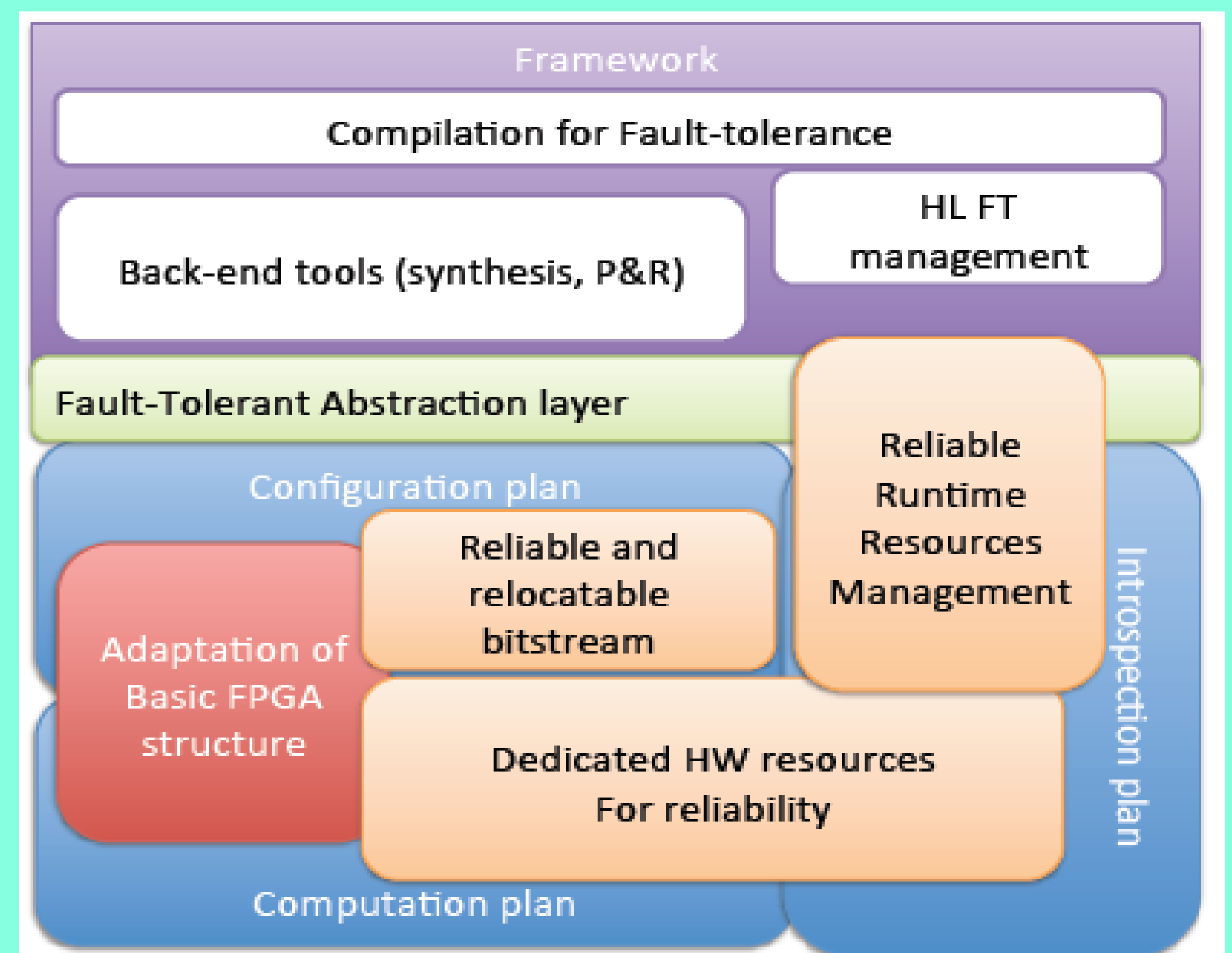


➤ Provides complete environment for the design of a fault tolerant and self-adaptable reconfigurable platform.



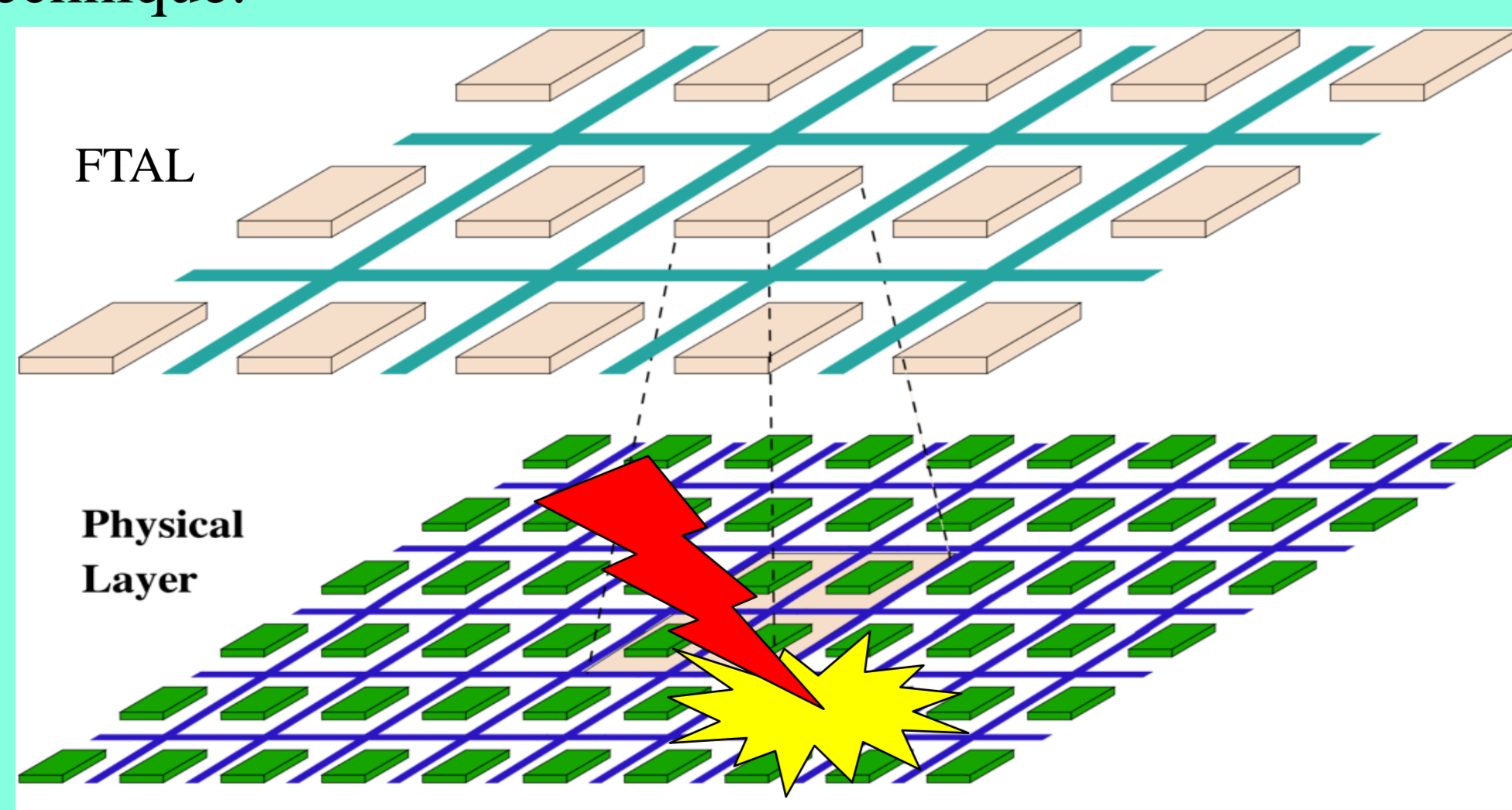
*ARDyT – Dynamically Reconfigurable Fault Tolerant Architecture

3 ARDyT : A Complete Framework



4 Health Monitoring Through FTAL

- FTAL, a virtual layer, monitors the health status of physical architecture.
- This Layer absorbs the hardware complexity of the mitigation technique.



*FTAL – Fault Tolerant Abstraction Layer

5 Conclusion

- Introduced framework for dynamically reconfigurable, fault tolerant SRAM based FPGA architecture.
- Proper sharing of mitigation strategies between different layers of architecture will enable to have a reliable solution at reasonable cost.

Prospective Work

- Functional specification of fault tolerant abstraction layer (FTAL), which includes,
 - Getting the fault detection responses from different hardware modules.
 - Run time resource management.
 - Task relocation upon detection of permanent error.
 - Dynamic partial reconfiguration of faulty module.

In association with,

