http://ardyt.irisa.fr/

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ARDyT: Architecture Reconfigurable Dynamique Tolérante

CONTEXT

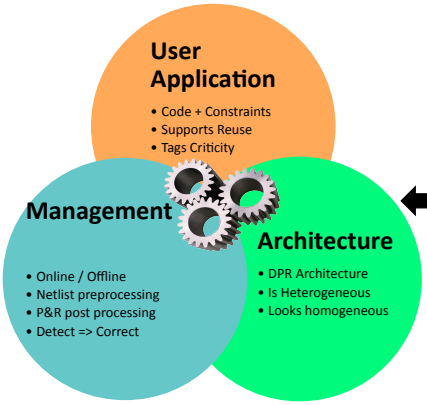
- In-the-field reconfiguration support makes FPGAs popular in embedded "evolvable platform"
- FPGAs are very sensitive to SEU if not using Rad-Hard technology
- Rad-Hard technologies suffer from several drawbacks

OBJECTIVES

- To provide a flexible, scalable and low cost reconfigurable hardware which exhibits fault tolerant capabilities and self healing features
- To address automotive and aerospace domains

	Rad Hard Technology	ARDyT
Time to market	−	+
Low cost	−	+
ITAR (International Traffic on Arms Regulation)	−	+
Fiability	+	−

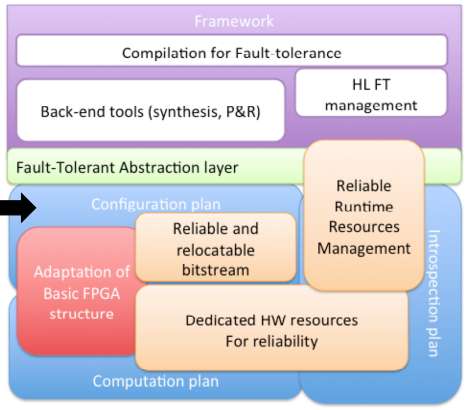
Stengths and weaknesses of the ARDyT proposal vs Rad-Hard approaches



Three axes: The designer is responsible for annotating the application; architecture and tools provide fault tolerant features

KEY PROPERTIES

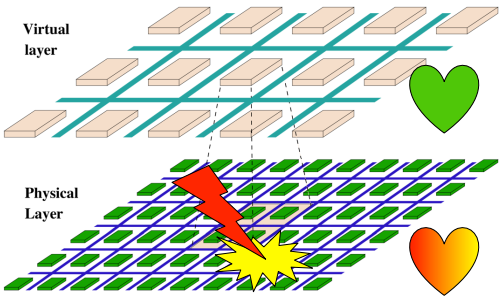
- ✓Global solution requires multiple levels
  - ✓Annotated User application
  - ✓Introspection compliant DPR Architecture
  - ✓Management facilities & policies
- ✓A fault tolerant abstraction layer gathers together these contributions
- ✓ARDyT supports on-demand and multi-level triplication mechanisms
- ✓Tools are made available early and drive the architecture



The Fault-Tolerant abstraction layer isolates tools from architecture hence favors reuse and concurrent development

EXPECTED RESULTS

- ✓ Parameterized cost-reliability tradeoff
- ✓ ITAR free platform
- ✓ Short time-to-market
- ✓ FTAL absorbs HW protection complexity
- ✓ Heterogeneous relocatable bitstream
- ✓ Labs for HW innovation



The global platform remains functional despite some SEU/ errors arise

FUTURE WORK

- ✓New HW primitives versus fault models
- ✓Hardware evolution based on a current Atmel FPGA
- ✓Adapting virtual layer generator to fit FT policies

PROJET FINANCÉ PAR L'ANR - PROJECT FUNDED BY THE ANR